K039-CW43-DW

IEEE802.11a/b/g/n/ac Wireless LAN With Bluetooth 5.0

Combo Stamp Module

DATASHEET

REV: 1.2

DATA: 28.11.2021

This specification may be changed with the improvement of the product. Please refer to the latest version of the usermanual.KERTONG reserves the right of final interpretation and modification of all contents of this specification.

Revision History

Date	Revision Content	Revised By	Version
2021/10/12	- Preliminary	LIU LEI	1.0
2021/10/18	- Pin Definition Modified	SHAWN	1.0
2021/11/28	- Modify RF Spec.	SHAWN	1.1

Contents

1. Introduction

1.1 About KERTONG

KERTONG Polytron Technologies Inc was established in Shenzhen in 2008. It is located in Xixiang, Shenzhen, Baoan. It is a high-tech enterprise specializing in the radio - related radio frequency series module application and the integrated solution platform of the products. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11a/b/g/n/ac 2x2 Access Points in the wireless LAN.

1.2 Product Overview

The wireless module complies with IEEE 802.11 a/b/g/n/ac 2x2 MIMO standard and it can achieve up to a speed of 433.3 Mbps*2 with dual stream in 802.11ac to connect the wireless LAN. The integrated module provides SDIO interface for Wi-Fi, UART / PCM interface for Bluetooth.

This K039-CW43-DW module using the chipset from CYPRESS's the CYW4373 with IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates of up to 433.3 Mbps. All rates specified in the IEEE 802.11a/b/g/n are supported. Included on-chip are 2.4 GHz and 5 GHz transmit amplifiers and receive low-noise amplifiers. Optional external PAs and LNAs are also supported. WLAN section supports the following host interface options: an SDIO v3.0 interface that can operate in 4b or 1b mode, a highspeed 4-wire UART, and a PCIe Gen1 (3.0 compliant) interface. The Bluetooth section supports a high-speed 4-wire UART interface.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

2.1 WLAN

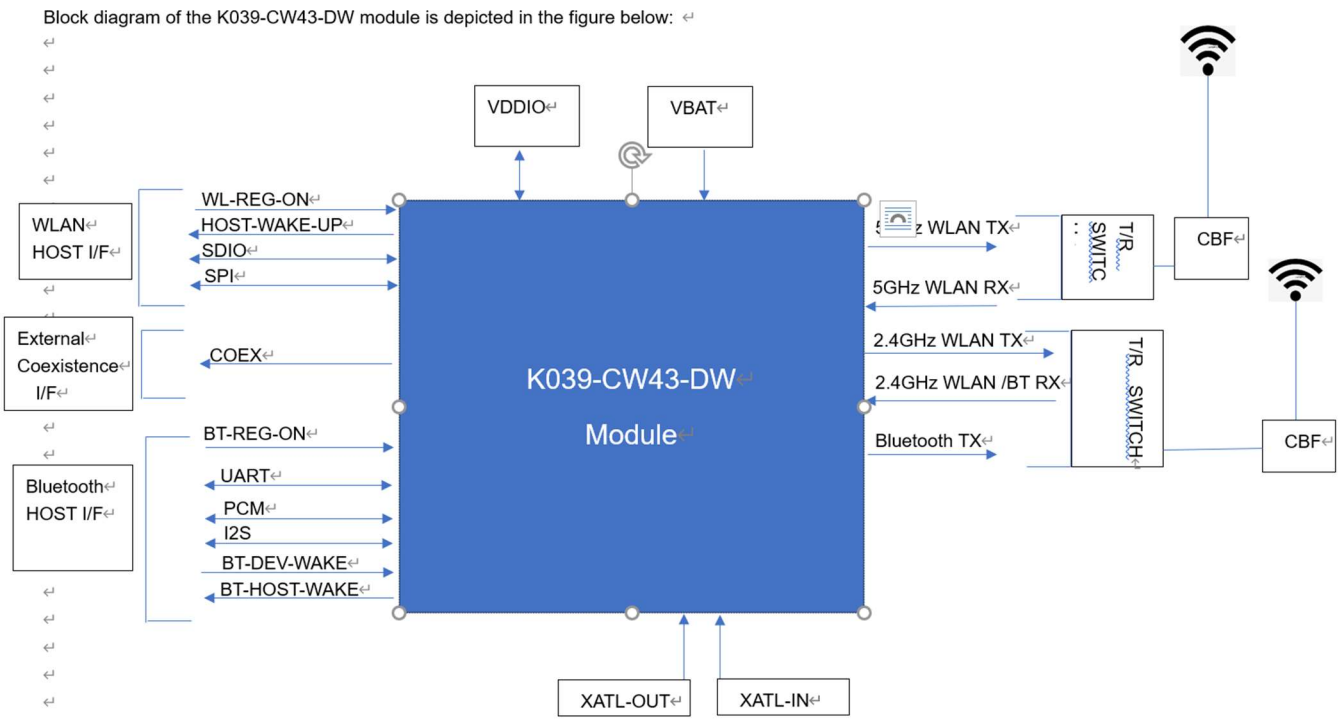
- IEEE 802.11a/b/g/n/ac dual-band radio with virtual-simultaneous dual-band operation
- Dual-stream spatial multiplexing up to 433.3 Mbps data rate.
- Lead Free design which is compliant with ROHS requirements.
- Supports 20, 40, 80 MHz channels with optional SGI(256 QAM modulation)
- Low power consumption and high performance
- Supports standard SDIO v3.0 and backward compatible with SDIO v2.0 host interfaces. - SDIO v3.0(4-bit) — up to 208 MHz clock rate in SDR104 mode
- Fully speed operation with Piconet and Scatternet support
- Backward compatible with SDIO v3.0 host interfaces
- PCIe mode complies with PCI Express base specification revision 3.0 compliant Gen1 interface for ×1 lane and power management base specification.
- SZIE：15mm * 13mm * 1.8(Max.)mm (L*W*H) LGA package

2.2 Bluetooth

- Complies with Bluetooth Core Specification Version 5.0 with provisions for supporting future specifications
- Simultaneous BT/ WLAN 2.4GHz(WL_ANT0) reception with a single antenna
- Simultaneous 5.8GHz (WL_ANT1) reception with a single antenna
- Enhanced Data Rate(EDR) compliant for both 2Mbps and 3Mbps supported
- Interface support, host controller interface (HCI) using a highspeed UART interface and PCM for audio data.
- BT UART (up to 4 Mbps) host digital interface that can be used concurrently with the above WLAN host interfaces.
- Aaptive frequency hopping (AFH) for reducing radio frequency interference.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.

2.4 Block Diagram

A simplified block diagram of the K039-CW43-DW module is depicted in the figure below:



3. Specification Table

3.1 General Specification

Major Chipset	Cypress CYW4373
Model Name	K039-CW43-DW
Product Description	Support WiFi/Bluetooth functionalities
Dimension	L x W x H: 15 x 13 x 1.8(Max.)mm
WiFi Host Interface	Support SDIO v2.0/v3.0
BT Interface	UART / PCM
Operating	-20°C to 80°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

3.2 Voltages (Absolute Maximum Ratings)

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5.6	V
WL_VIO_SD	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.8	V

3.3 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.8	V
VDDIO	1.71	-	3.63	V

※NOTE: The K039-CW43-DW module requires two power supplies: VBAT and VDD

3.4 ESD Sensitivity

Human Body Model

MODEL:HBM	ESD SENSITIVITY PASS:2000V		V CLASS: 2
PIN COMBINATION	SAMPLE SIZE	PASSED VOLTS	NOTE: FOR EIAJ TEST NO CLASSIFICATION CLASS 0: < 250V CLASS 1A: 250V TO 499V CLASS 1B: 500V TO 999V CLASS 1C: 1000V TO 1999V CLASS 2: 2000V TO 3999V CLASS 3A: 4000V TO 7999V CLASS 3B: ≧8000V
VDD (+)	2	+2000V	
VDD (-)	2	-2000V	
GND (+)	2	+2000V	
GND (-)	2	-2000V	
IO (±)	2	±2000V	

SDM/CDM (Socket/Charge Device Model)

MODEL:SDM	ESD SENSITIVITY PASS:200V		V CLASS: II
PIN COMBINATION	SAMPLE SIZE	PASSED VOLTS	NOTE: FOR EIAJ TEST NO CLASSIFICATION CLASS I: <200V CLASS II: 200V TO <500V CLASS III: >500V TO <1000V CLASS IV: >1000V
VDD (+)	2	+500V	
VDD (-)	2	-225V	
GND (+)	2	+500V	
GND (-)	2	-200V	
IO (±)	2	+225V	

3.5 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description	
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant	
Frequency Range	2.400 GHz ~ 2.483 GHz (2.4 GHz ISM Band)	
Channels	2.4GHz：Ch1 ~ Ch11 (by software to setting country code)	
	2.4GHz：Ch1 ~ Ch13 (by software to setting country code) default	
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK	
Output Power	802.11b /CCK: 16 dBm ± 1.5 dB @ EVM ≤ -9dB	
	802.11g //64-QAM(R=3/4) : 15 dBm ± 1.5 dB @ EVM ≤ -25dB	
	802.11n /802.11n /64-QAM(R=5/6) : 14 dBm ± 1.5 dB @ EVM ≤ -27dB	
(20MHz) **Receive Sensitivity (11n) @10% PER**	- MCS=0	PER @ -88 dBm, typical
	- MCS=1	PER @ -84 dBm, typical
	- MCS=2	PER @ -82 dBm, typical
	- MCS=3	PER @ -80 dBm, typical
	- MCS=4	PER @ -77 dBm, typical
	- MCS=5	PER @ -73 dBm, typical
	- MCS=6	PER @ -71 dBm, typical
	- MCS=7	PER @ -68 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps	PER @ -89 dBm, typical
	- 9Mbps	PER @ -87 dBm, typical
	- 12Mbps	PER @ -87 dBm, typical
	- 18Mbps	PER @ -85 dBm, typical
	- 24Mbps	PER @ -83 dBm, typical
	- 36Mbps	PER @ -79 dBm, typical
	- 48Mbps	PER @ -75 dBm, typical
	- 54Mbps	PER @ -72 dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps	PER @ -94 dBm, typical
	- 2Mbps	PER @ -89 dBm, typical
	- 5.5Mbps	PER @ -87 dBm, typical
	- 11Mbps	PER @ -85 dBm, typical
(40MHz)	- MCS=0	PER @ -88 dBm, typical
	- MCS=1	PER @ -84 dBm, typical

Receive Sensitivity (11n)	- MCS=2	PER @ -82 dBm, typical
	- MCS=3	PER @ -80 dBm, typical
@10% PER	- MCS=4	PER @ -76 dBm, typical
	- MCS=5	PER @ -74 dBm, typical
	- MCS=6	PER @ -72 dBm, typical
	- MCS=7	PER @ -67 dBm, typical
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	
Antenna Type	2.4~2.4835GHz: Dipole Antenna with 0~2 dBi peak gain	

3.6 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description	
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant	
Frequency Range	5.15GHz ~ 5.845 GHz (5GHz UN-II Band)	
Channels	5.15GHz~5.25GHz (5180, 5200,5220,5240) 5.25GHz~5.35GHz (5260,5280,5300,5320) 5.5GHz~5.7GHz (5500,5520,5540,5560,5580,5600,5620,5640,5660,5680,5700) 5.725GHz~5.845GHz (5745,5765,5785,5805,5825)	
Modulation	802.11a : OFDM/ 64-QAM ,16-QAM, QPSK, BPSK 802.11n : DQPSK, DBPSK, CCK 802.11ac: OFDM/ 256-QAM	
	802.11a /54Mbps: 13 dBm ± 1.5 dB @ EVM ≤ -25dB	
	802.11n /MCS7 : 12 dBm ± 1.5 dB @ EVM ≤ -27dB	
	802.11ac /MCS9: 10 dBm ± 1.5 dB @ EVM ≤ -32dB	
(20MHz) **Receive Sensitivity (11n) @10% PER**	- MCS=0	PER @ -90 dBm, typical
	- MCS=1	PER @ -88 dBm, typical
	- MCS=2	PER @ -86 dBm, typical
	- MCS=3	PER @ -83 dBm, typical
	- MCS=4	PER @ -77 dBm, typical
	- MCS=5	PER @ -73 dBm, typical
	- MCS=6	PER @ -72 dBm, typical
	- MCS=7	PER @ -69 dBm, typical

(20MHz) **Receive Sensitivity (11g)** **@10% PER**	- 6Mbps	PER @ -90dBm, typical
	- 9Mbps	PER @ -88 dBm, typical
	- 12Mbps	PER @ -86 dBm, typical
	- 18Mbps	PER @ -85 dBm, typical
	- 24Mbps	PER @ -81 dBm, typical
	- 36Mbps	PER @ -79 dBm, typical
	- 48Mbps	PER @ -75 dBm, typical
	- 54Mbps	PER @ -72 dBm, typical
(40MHz) **Receive Sensitivity (11n)** **@10% PER**	- MCS=0	PER @ -87 dBm, typical
	- MCS=1	PER @ -85 dBm, typical
	- MCS=2	PER @ -83 dBm, typical
	- MCS=3	PER @ -78 dBm, typical
	- MCS=4	PER @ -76 dBm, typical
	- MCS=5	PER @ -71 dBm, typical
	- MCS=6	PER @ -69 dBm, typical
	- MCS=7	PER @ -68 dBm, typical
（20MHz) **Receive Sensitivity (11ac)** **@10% PER**	- MCS=0	PER @ -89 dBm, typical
	- MCS=1	PER @ -87 dBm, typical
	- MCS=2	PER @ -84 dBm, typical
	- MCS=3	PER @ -81 dBm, typical
	- MCS=4	PER @ -79 dBm, typical
	- MCS=5	PER @ -76 dBm, typical
	- MCS=6	PER @ -72 dBm, typical
	- MCS=7	PER @ -71 dBm, typical
	- MCS=8	PER @ -68 dBm, typical
（40MHz) **Receive Sensitivity (11ac)** **@10% PER**	- MCS=0	PER @ -86 dBm, typical
	- MCS=1	PER @ -82 dBm, typical
	- MCS=2	PER @ -80 dBm, typical
	- MCS=3	PER @ -77 dBm, typical
	- MCS=4	PER @ -76 dBm, typical
	- MCS=5	PER @ -71 dBm, typical
	- MCS=6	PER @ -68 dBm, typical
	- MCS=7	PER @ -66 dBm, typical
	- MCS=8	PER @ -64 dBm, typical
	- MCS=9	PER @ -62 dBm, typical
	- MCS=0	PER @ -81 dBm, typical
	- MCS=1	PER @ -79 dBm, typical

（80MHz) Receive Sensitivity (11ac) @10% PER	- MCS=2	PER @ -77 dBm, typical
	- MCS=3	PER @ -75 dBm, typical
	- MCS=4	PER @ -71 dBm, typical
	- MCS=5	PER @ -68 dBm, typical
	- MCS=6	PER @ -65 dBm, typical
	- MCS=7	PER @ -61 dBm, typical
	- MCS=8	PER @ -59 dBm, typical
	- MCS=9	PER @ -59 dBm, typical
Maximum Input Level	802.11a/n : -20 dBm	
	802.11ac : -30 dBm	
Antenna Type	5180 ~5240MHz: Dipole Antenna with 3 dBi peak gain	
	5260 ~5320MHz: Dipole Antenna with 3 dBi peak gain	
	5500 ~5700MHz: Dipole Antenna with 3 dBi peak gain	
	5745 ~5805MHz: Dipole Antenna with 2 dBi peak gain	

5GHz(20MHz) Channel table

Band (GHz)	Operating Channel Numbers	Channel center frequencies(MHz
5.15GHz~5.25GHz	36	5180
	40	5200
	44	5220
	48	5240
5.25GHz~5.35GHz	52	5260
	56	5280
	60	5300
	64	5320
5.5GHz~5.7GHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
	140	5700
5.725GHz~5.845GHz	149	5745
	153	5765
	157	5785
	161	5805
	165	5825

※NOTE: Channel Table

3.7 Bluetooth Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

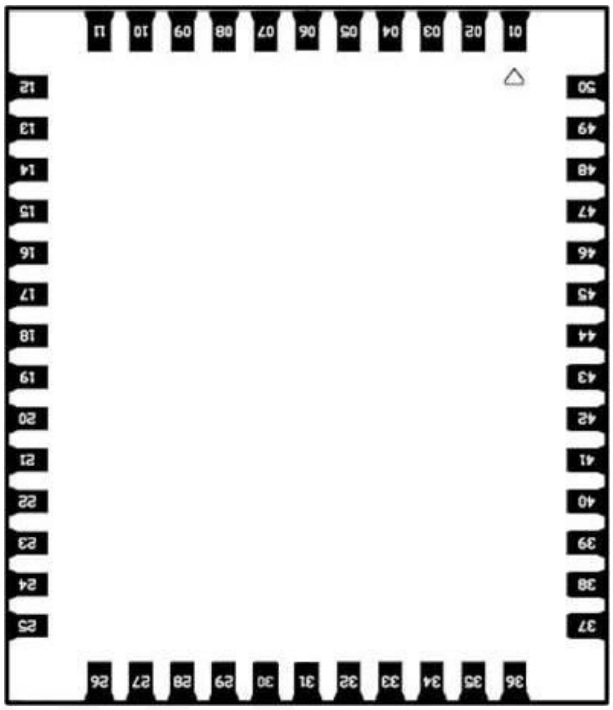
Feature	Description		
Bluetooth Standard	Bluetooth V5. 0 and UP to 4 Mbps.		
QDID Number			
Declaration ID			
Host Interface	UART		
Antenna Reference	Antennas with 0~2 dBi peak gain		
Frequency Band	2402MHz ~ 2480MHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
	Min.	**Typical.**	**Max.**
Output Power		8 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-88 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-91 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-87 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

※NOTE: Output power can be configured by HCD firmware

4. Pin Assignments

4.1 Pin Map

< TOP VIEW >



4.2 Pin Table

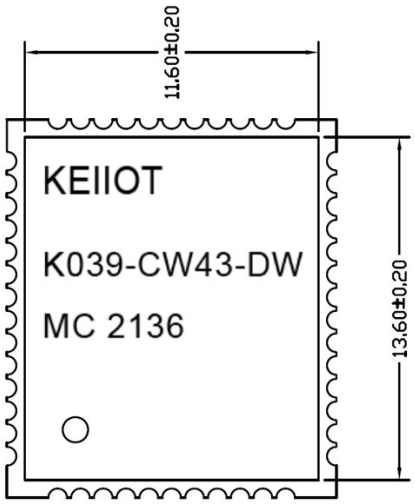
NO	Name	Type	Description
1	GND	—	Ground connections
2	WL/BT_ANT0	I/O	RF I/O port0
3	GND	—	Ground connections
4	GND	—	Ground connections
5	GND	—	Ground connections
6	GND	—	Ground connections
7	GND	—	Ground connections
8	GND	—	Ground connections
9	WL_ANT1	I/O	RF I/O port1
10	GND	—	Ground connections
11	GND	—	Ground connections
12	NC	—	No connect
13	XTAL_OUT	O	External Crystal out

14	XTAL_IN	I	External Crystal in/ Single clock source in
15	WL_REG_ON	I	Low asserting reset for WiFi core
16	WL_HOST_WAKE	O	WLAN to wake-up HOST
17	SDIO_DATA_CMD	I/O	SDIO command line
18	SDIO_DATA_CLK	I/O	SDIO clock line
19	SDIO_DATA_3	I/O	SDIO data line 3
20	SDIO_DATA_2	I/O	SDIO data line 2
21	SDIO_DATA_0	I/O	SDIO data line 0
22	SDIO_DATA_1	I/O	SDIO data line 1
23	GND	—	Ground connections
24	NC	—	No connect
25	VIN_LDO	P	Internal Buck voltage generation pin
26	VIN_LDO_OUT	P	Internal Buck voltage generation pin
27	PCM_SYNC	I/O	PCM sync signal
28	PCM_IN	I	PCM data input
29	PCM_OUT	O	PCM Data output
30	PCM_CLK	I/O	PCM clock
31	LPO	I	External Low Power Clock input (32.768KHz)
32	GND	—	Ground connections
33	NC	—	No connect
34	VDDIO	P	I/O Voltage supply input
35	NC	—	No connect
36	VBAT	P	Main power voltage source input
37	NC	—	No connect
38	BT_REG_ON	I	Low asserting reset for Bluetooth core
39	GND	—	Ground connections
40	UART_TXD	O	Bluetooth UART interface
41	UART_RXD	I	Bluetooth UART interface
42	UART_RTS_N	O	Bluetooth UART interface
43	UART_CTS_N	I	Bluetooth UART interface
44	NC	—	No connect
45	NC	—	No connect
46	NC	—	No connect
47	NC	—	No connect
48	NC	—	No connect
49	BT_WAKE	I	HOST wake-up Bluetooth device
50	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST

5. Mechanical and Layout Design

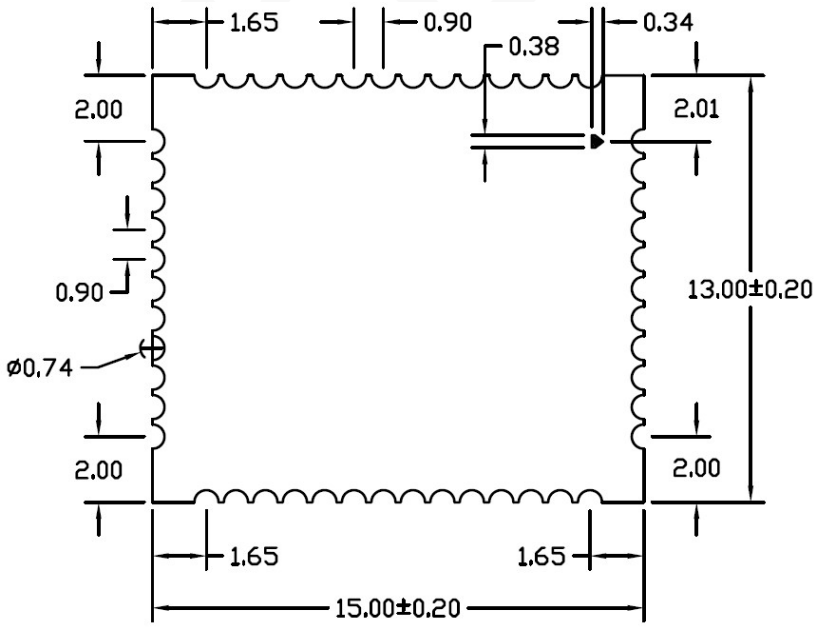
※NOTE (Unit:mm)

< TOP VIEW >



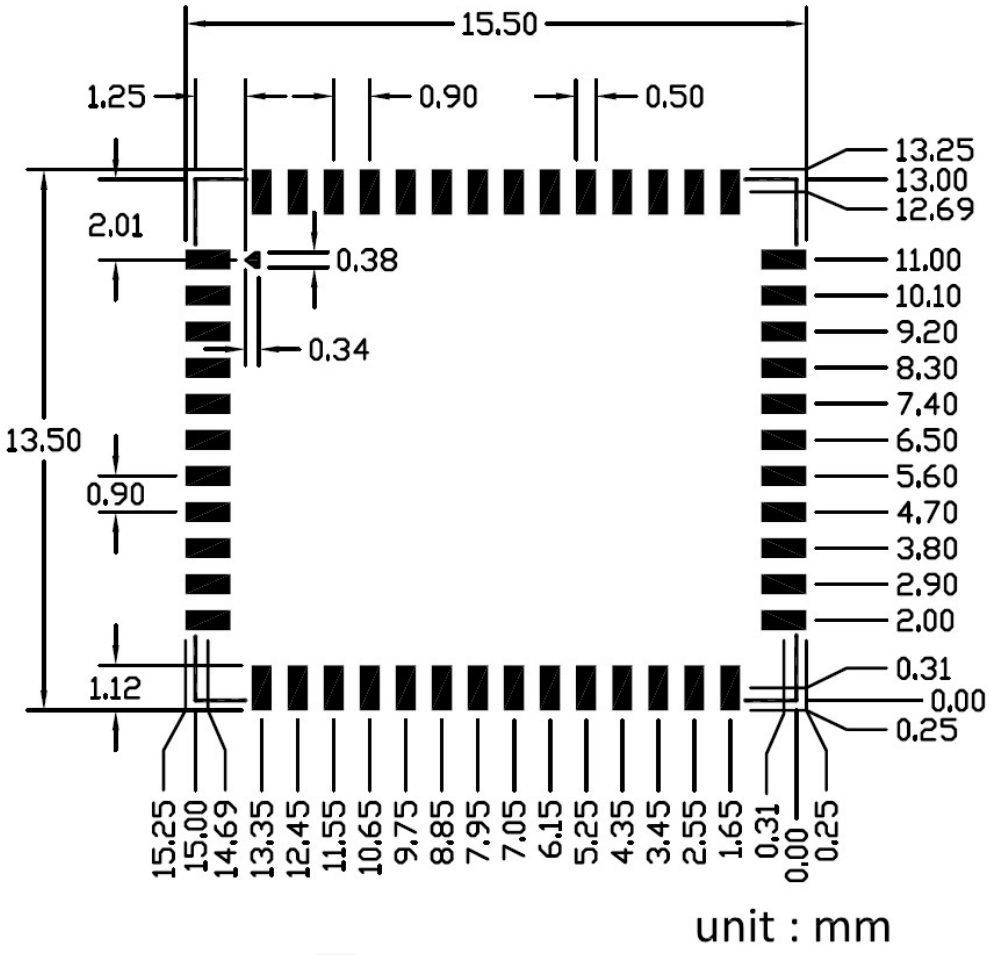
< Side View >

< Bottom VIEW >



Layout Recommendation

< Top VIEW >



6. Frequency References

6.1 External Clock Reference

The module uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

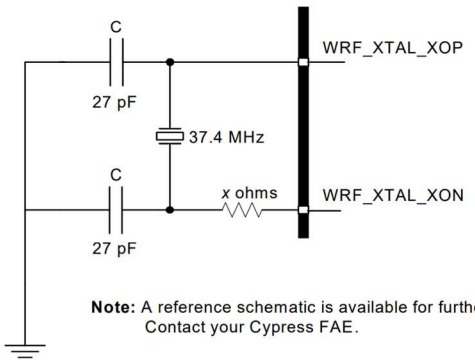
External LPO signal characteristics:

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±20	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave or sine wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<10,000	ppm
Output high voltage	0.7Vio - Vio	V

External LPO signal characteristics:

The CYW4373 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 5. Consult the reference schematics for the latest configuration.

Figure 5. Recommended Oscillator Configuration



Note: A reference schematic is available for further details. Contact your Cypress FAE.

6.2 SDIO v3.0 and SDIO v2.0

The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps),SDR104(208MHz) and DDR50(50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided. including the new UHS-I modes:

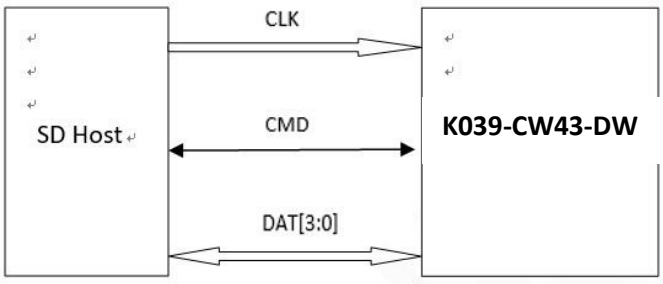
- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3 V signaling).
- HS: High speed up to 50 MHz (3.3 V signaling).
- SDR12: SDR up to 25 MHz (1.8 V signaling).
- SDR25: SDR up to 50 MHz (1.8 V signaling).
- SDR50: SDR up to 100 MHz (1.8 V signaling).
- SDR104: SDR up to 208 MHz (1.8 V signaling)
- DDR50: DDR up to 50 MHz (1.8 V signaling).

※**Note:** The K039-CW43-DW is backward compatible with SDIO v2.0 host interfaces.

SDIO PIN Descriptions

SD 4-Bit Mode	
DATA0	Data line 0
DATA1	Data line 1 or Interrupt
DATA2	Data line 2 or Read Wait
DATA3	Data line 3
CLK	Clock
CMD	Command line

Signal Connections to SDIO Host



7. Interface Timing Diagram

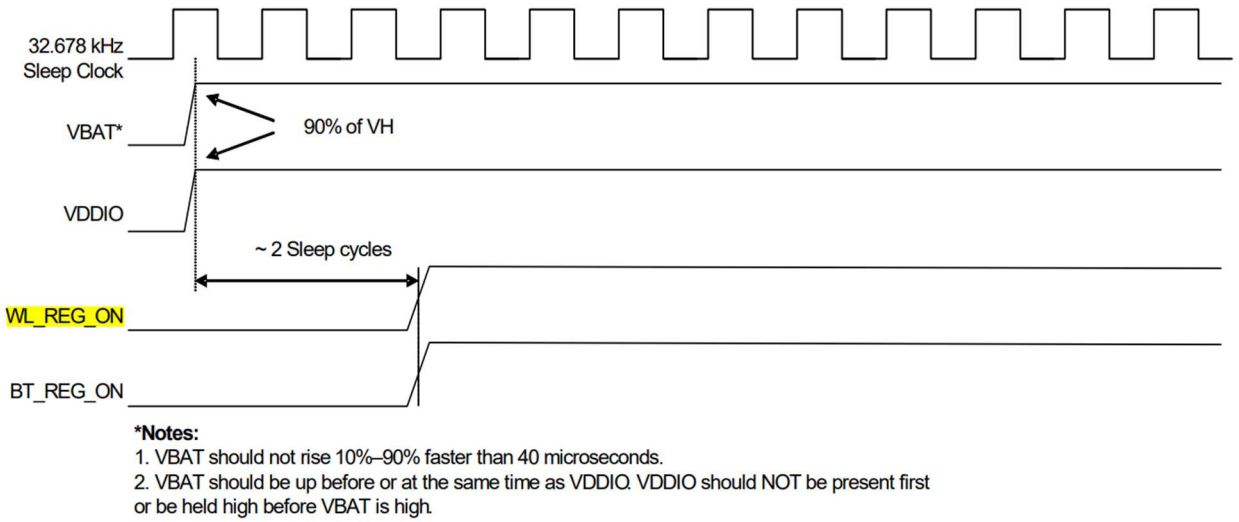
7.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.

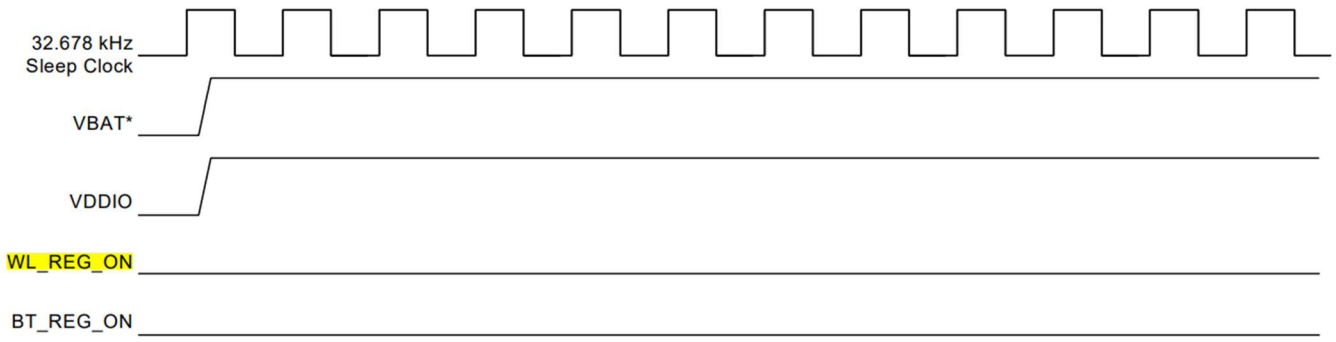
※ BT_RST_N: Low asserting reset for Bluetooth only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).

Figure 44. WLAN = ON, Bluetooth = ON



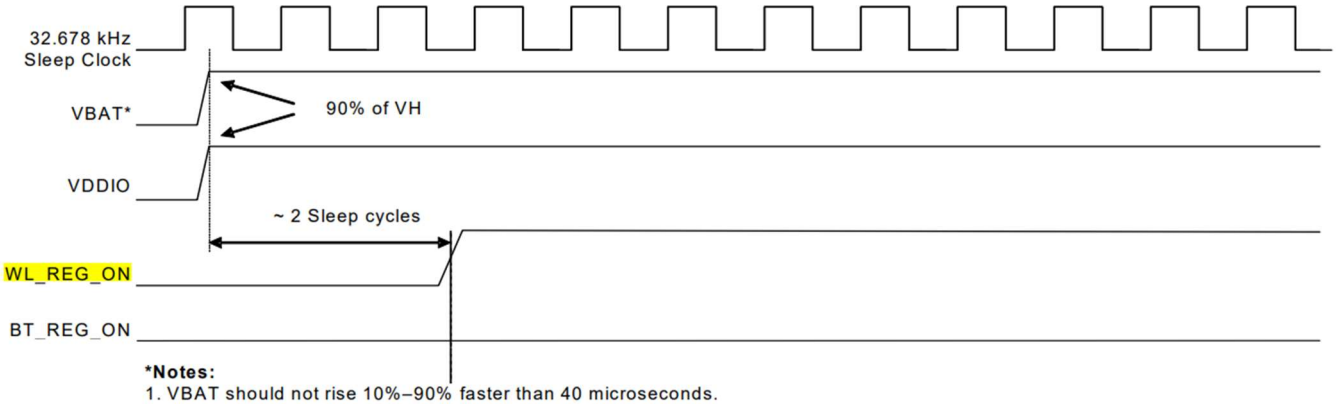
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=ON, Bluetooth=ON



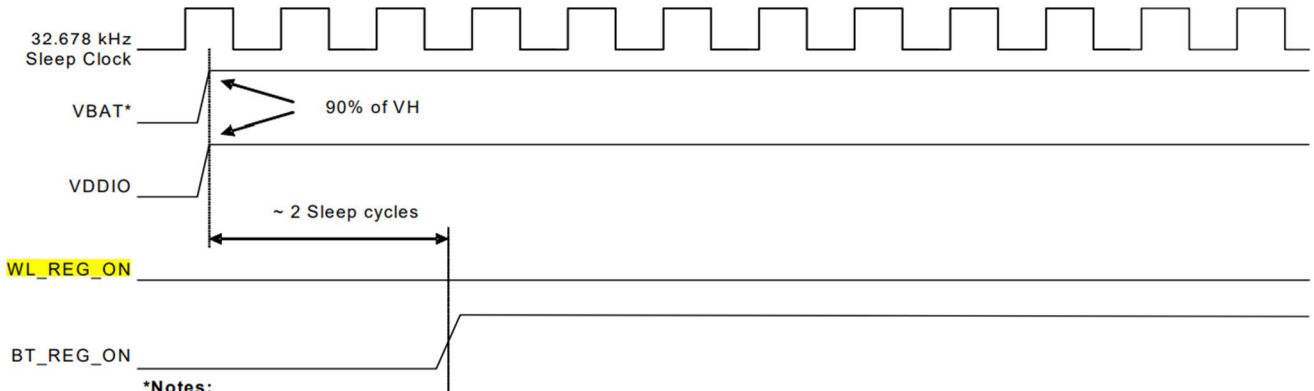
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=OFF, Bluetooth=OFF



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

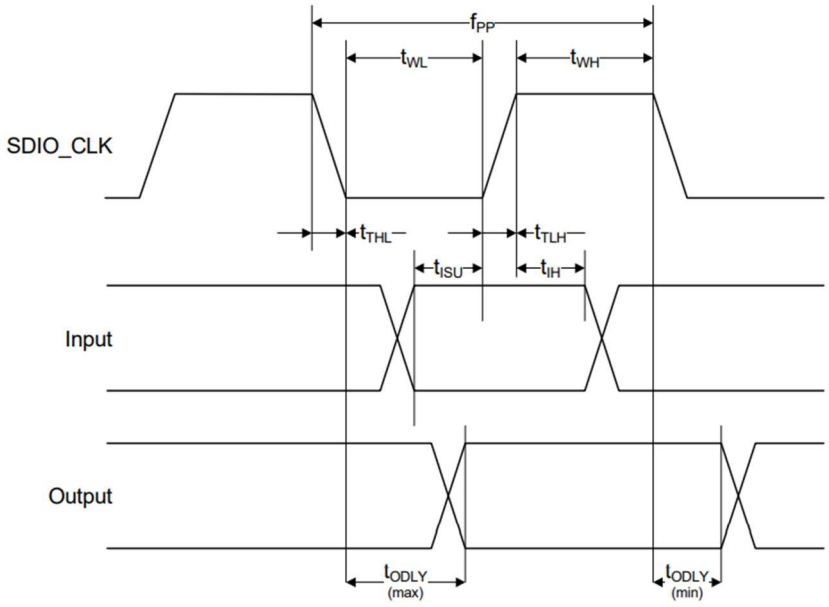
WLAN=ON, Bluetooth=OFF



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=OFF, Bluetooth=ON

7.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

1. Timing is based on CL ≤ 40 pF load on CMD and Data.
2. Min (VIH) = 0.7 × VDDIO and max (VIL) = 0.2 × VDDIO.

7.3 SDIO Bus Timing Specifications in SDR Modes

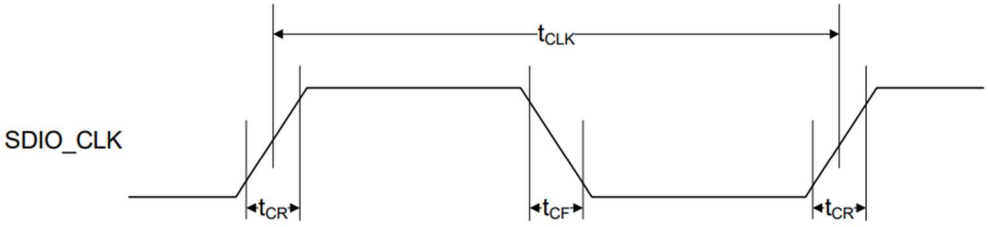


Table 53. SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @ 100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @ 208 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	30	70	%	–

Card Input Timing

Figure 38. SDIO Bus Input Timing (SDR Modes)

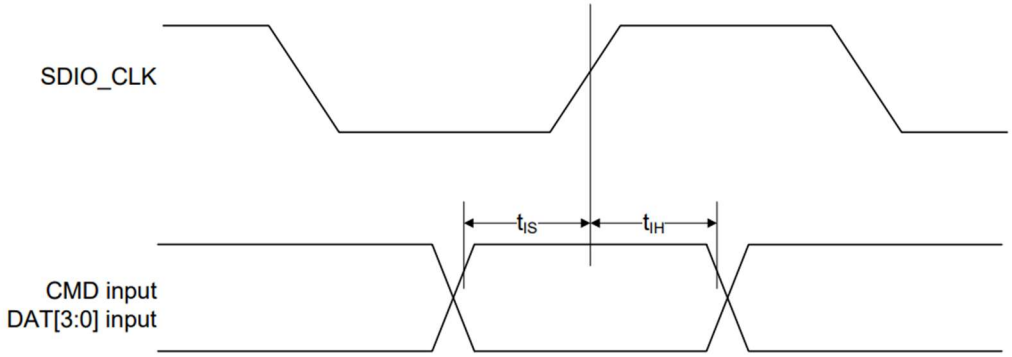


Table 54. SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Min	Max	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

Card Output Timing

Figure 39. SDIO Bus Output Timing (SDR Modes up to 100 MHz)

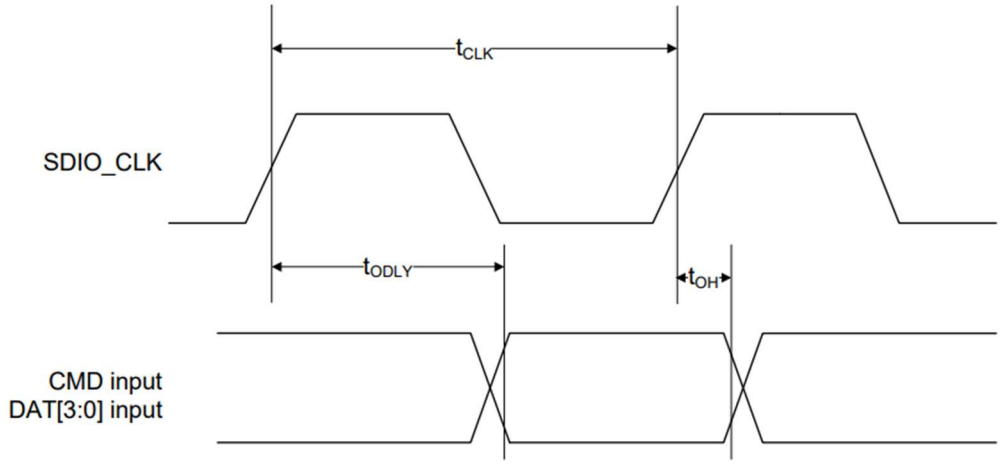
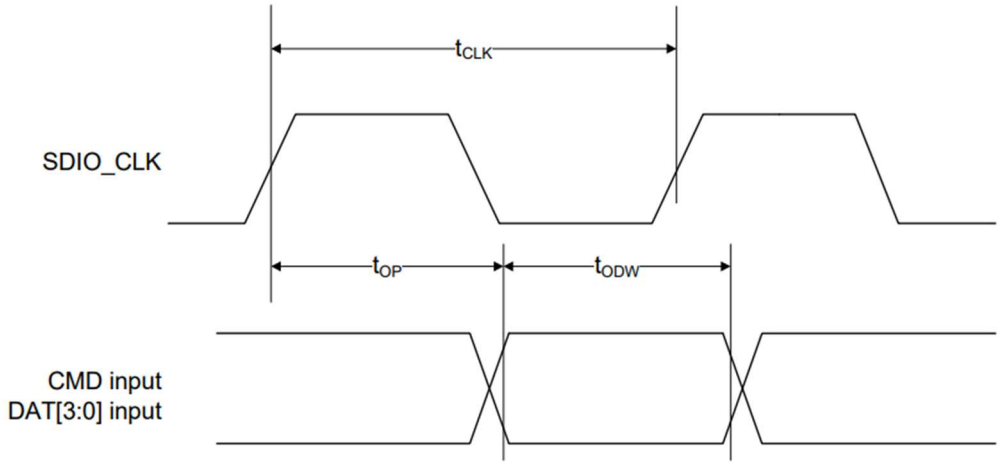


Table 55. SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	Min	Max	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK} ≥ 10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L= 15 pF

Figure 40. SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)



7.4 SDIO High Speed Mode Timing Diagram

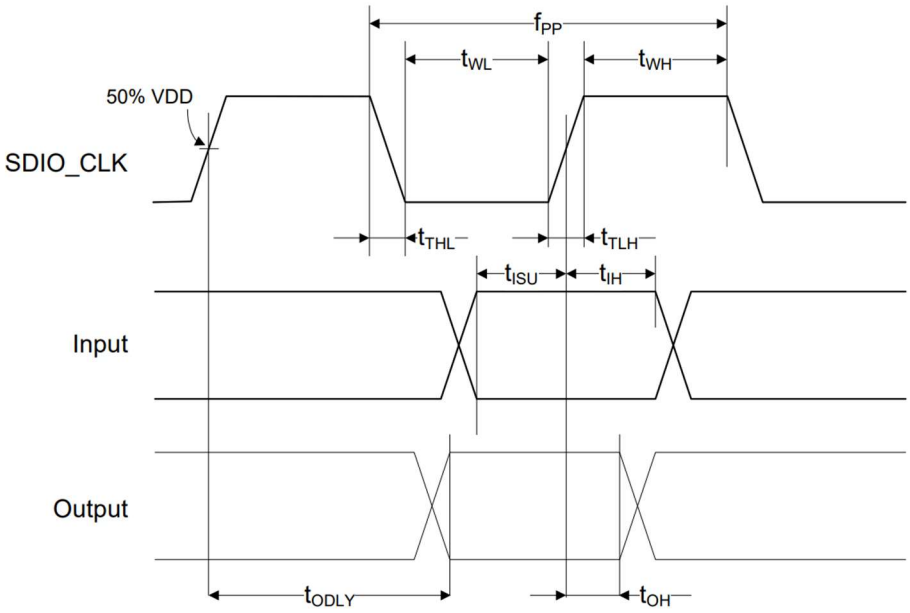


Table 52. SDIO Bus Timing[1] Parameters (High-Speed Mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)	–	–	–	–	–
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)	–	–	–	–	–
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

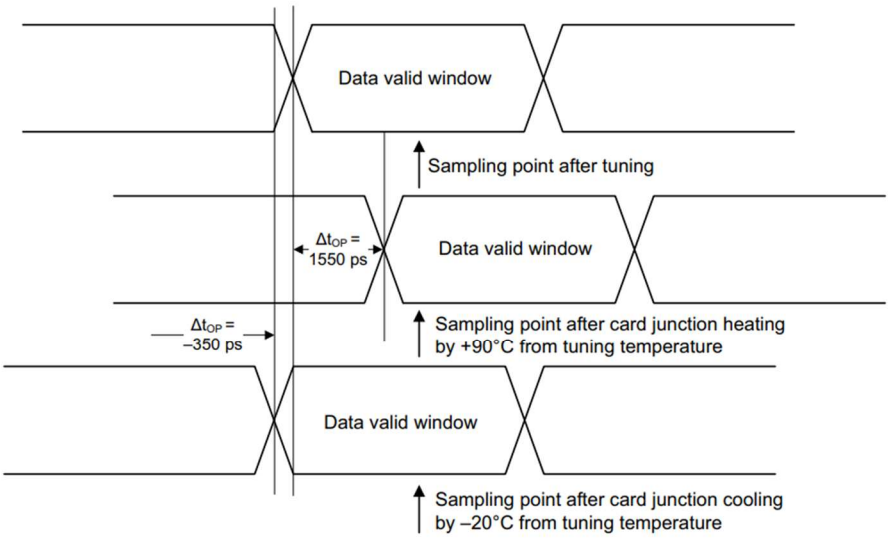
1. Timing is based on CL ≤ 40 pF load on CMD and Data.
2. Min (VIH) = 0.7 × VDDIO and max (VIL) = 0.2 × VDDIO.

Table 56. SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	Min	Max	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW} = 2.88 ns @ 208 MHz

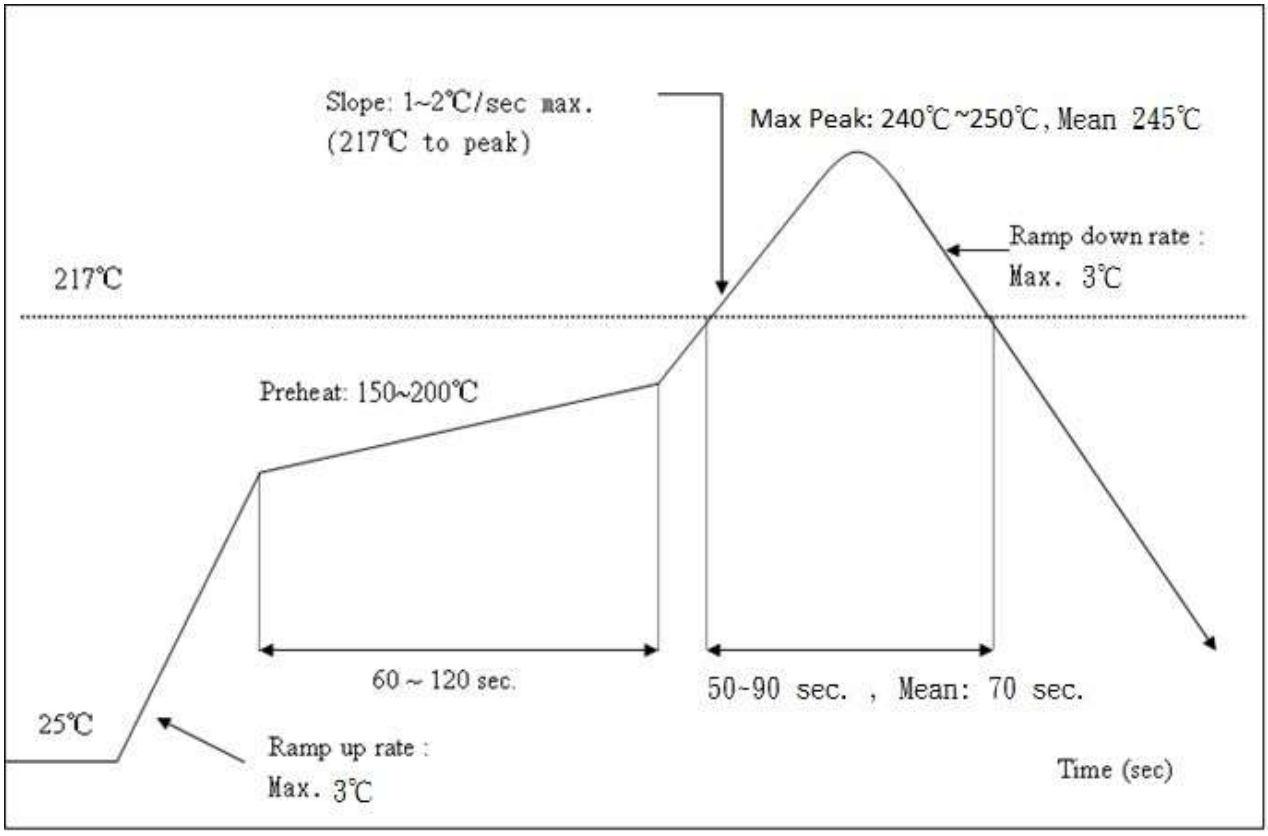
- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90°C during operation.
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20°C during operation.
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20°C to +125°C during operation.

Figure 41. Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)



8. Recommended Reflow Profile

Referred to IPC/JEDEC standard.
Peak Temperature :<250°C Number
of Times : ≤2 times



ENVIRONMENTAL.
Operating :
※Operating Temperature: -10°C to +70 °C
※Relative Humidity: 5-90% (non-condensing)

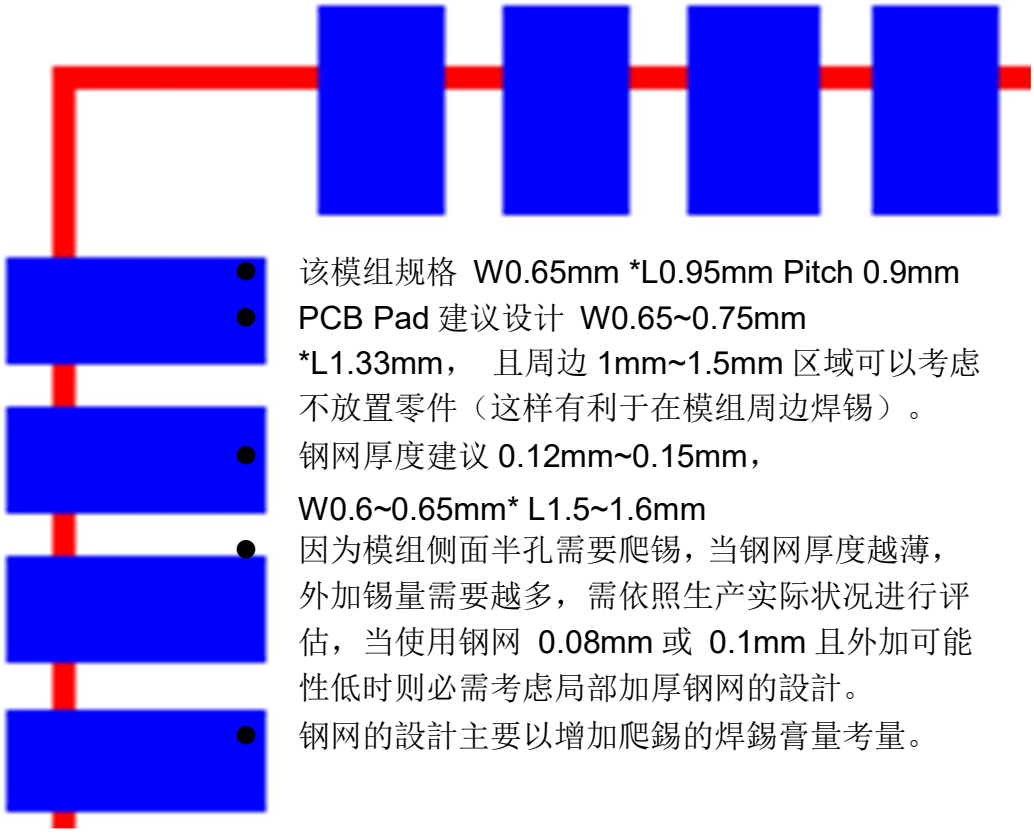
Storage
※Temperature: -40°C to +80°C (non-operating)
※Relevant Humidity: 5-95% (non-condensing)

MTBF caculation
※Over 150,000hour

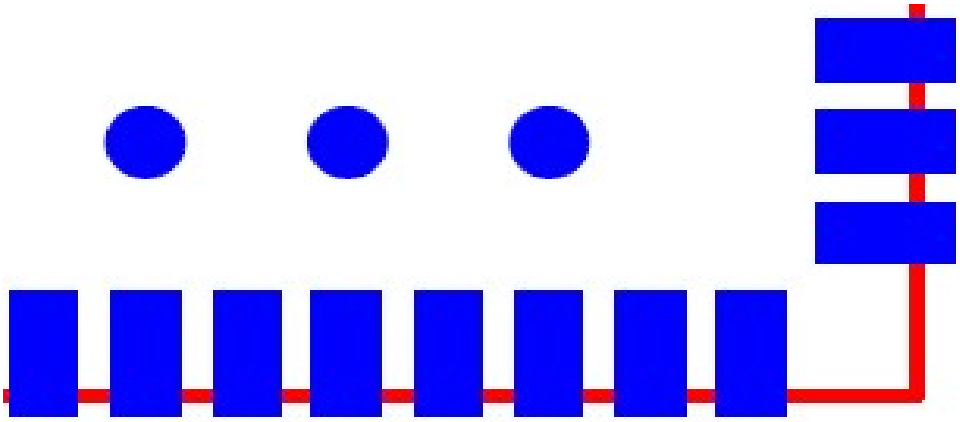
The aperture of stencil should be larger than foot print of module, and the stencil thickness should be not less than 0.12mm.

NOTE: it must use N2 for reflow and suggest the coneentration of oxygenless than 5000 ppm

9. PCB Layout Solder Paste



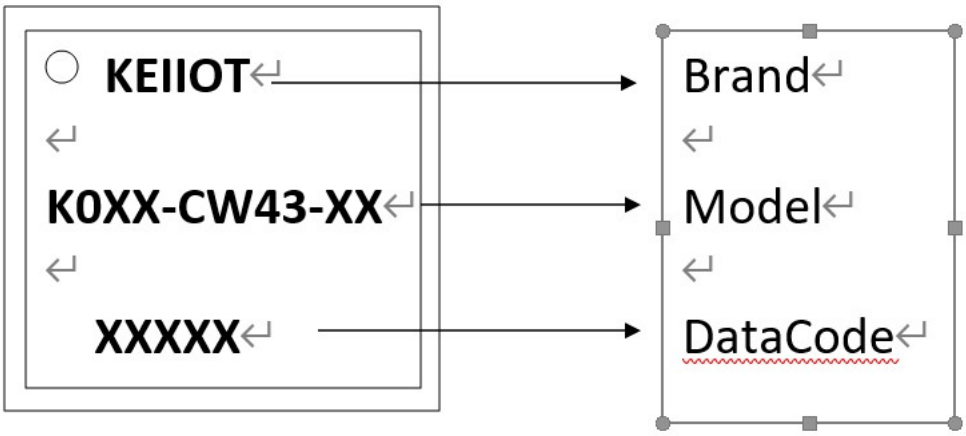
- Module Specifications : W:0.65mm * L:0.95mm pitch 0.9 mm
- The proposed design W:0.65~0.75 mm * L:1.33mm. Consider not place other parts in the peripheral area of 1 mm ~ 1.5 mm to facilitate additional amount of solder for PCB pad.
- We Suggest the thickness of Stencil between 0.12 mm ~0.15mm, the W between 0.6~0.65mm and the L between L1.5~1.6mm.
- If the thickness of the stencil is thinner, we suggest to adding more solder, to increase the wetting ability. Depends on different production situation, if the stencil thickness is 0.08~0.1mm, and the module nearby area is no more space for expending soldering area, we will suggest to increase the stencil thickness to increase the wetting ability.
- The major consideration parts of stencil design is to increase the solder paste wetting ability.

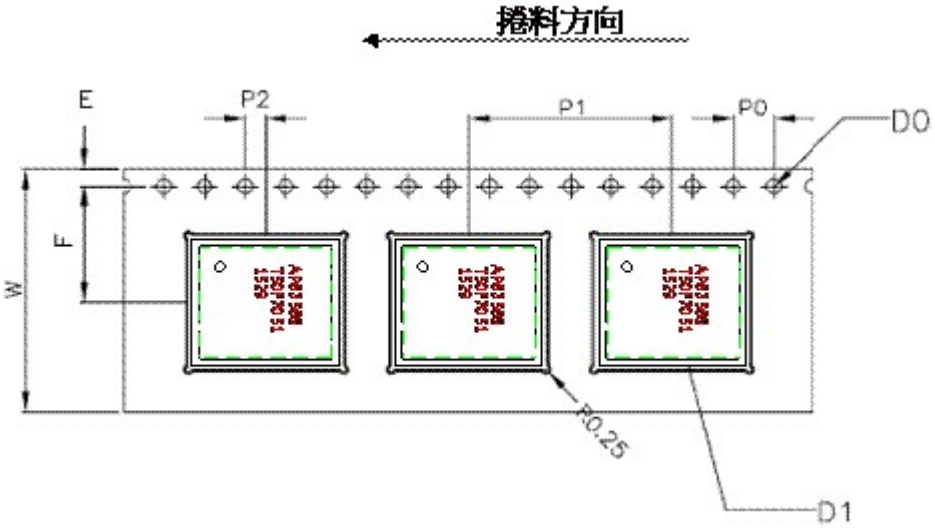


该模组规格 L 0.7mm
PCB Pad 设计 L 0.8mm 钢网
建议开 L0.5mm~0.6mm 然后
适当内缩，这样可以避免浮高
造成高度影响。

- Module Specifications L 0.7mm
- The design for PCB Pad : L:0.8mm
- We recommend the apertures for stencil L:0.5mm~0.6mm
- In order to avoid highness impact caused solder paste thickness, the stencil open size can be appropriately retracted

10. Package Information





W	24.00±0.30
A0	15.30±0.10
B0	13.30±0.10
K0	2.00±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	20.00±0.10
P2	2.00±0.10
D0	1.50 +0.10 -0.00
D1	ø1.5OMIN

1> 10 sprocket hole pitch cumulative tolerance ±0.20.

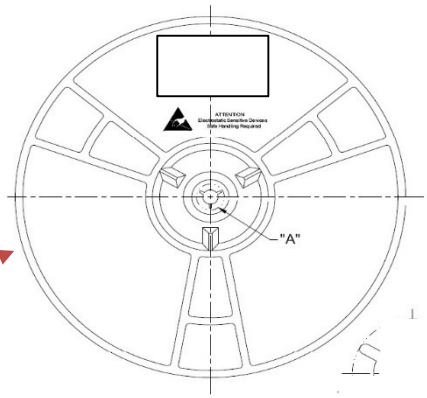
2> Carrier camber is within 1 mm in 250 mm.

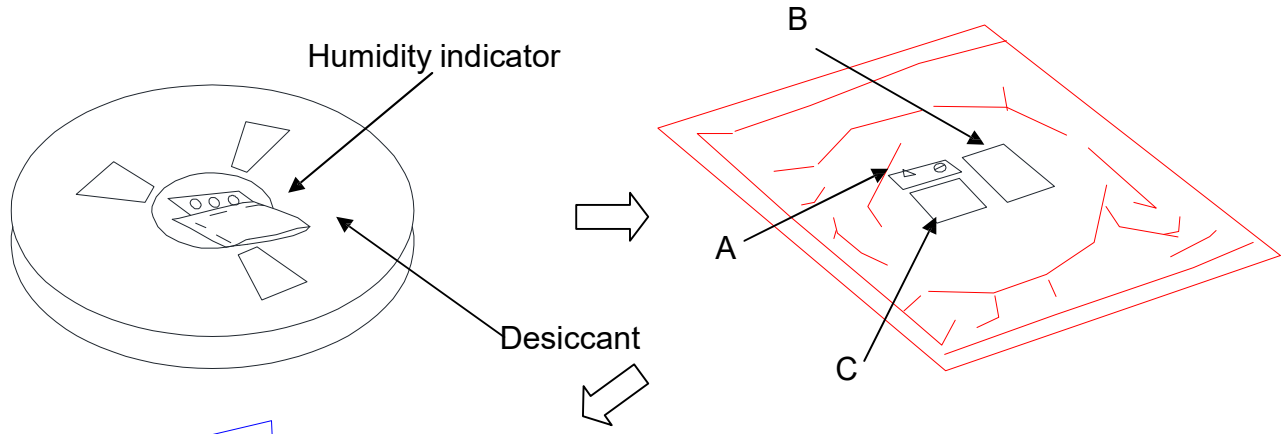
3> Material : Black Conductive Polystyrene Alloy.

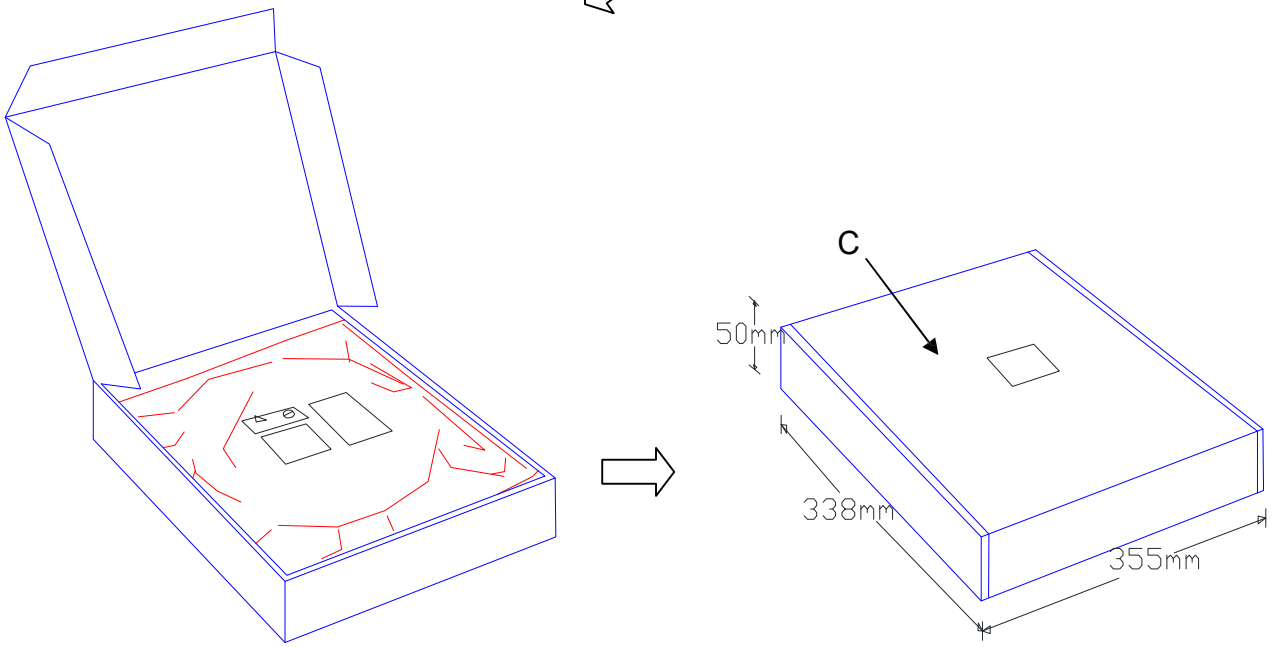
4> All dimensions meet EIA-481-D requirements.

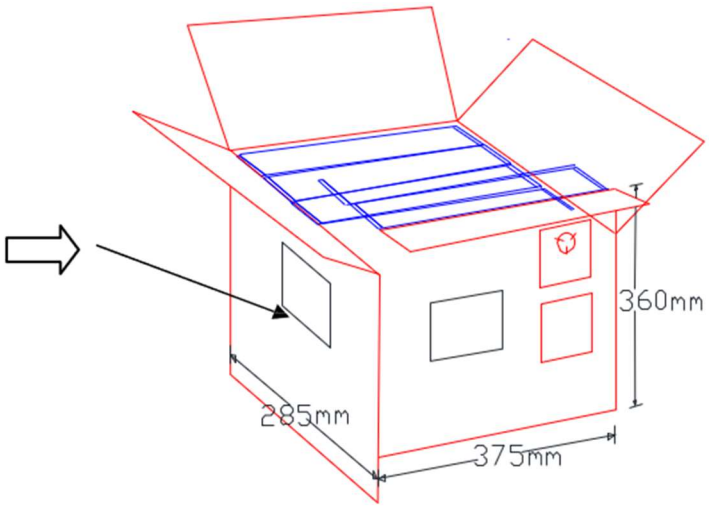
5> Thickness : 0.30±0.05mm.

6> Component load per 13”reel : 1,000 pcs/packing









11. This product is RoHS compliance

Wireless module before the SMT Note:

When customers Open stencil must be sure the hole bigger to the Wireless module plate, please press 1 to 1 and 0.7 mm is widened to open outward, the thickness of 0.12 mm.

① Can't get the wifi module bare hands when needs,must we wear the gloves and static ring.

The furnace temperature according to the size of the customer the mainboard ,generally like to stick on a tablet standard temperature of 250 + - 5,can do 260 + - 5. Storage and use Wifi module control should pay attention to the following matters:

① Module of the storage life of vacuum packaging：

1-1. Storage life：12 months. Storage conditions:<40 . Relative ℃ humidity:<90%R.H.

1-2. 1-2.After this bag is opened , devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing must be

1-3. Check the humidity card :stored at ≦20%RH.If :30%~40%(pink)or greater than 40%(red).Labeling module has moisture absorption.

① Mounthed within 168 hours at factory conditions of: ≦ ℃t 30% ， ≦60%R.H.

② Once opened, the workshop the preservation of life for 168 hours.

1-4. If baking is required,devices may be baked for:

① Modules must be to remove module moisture problem.

② Baking temperature: 125 , 8 hours. ℃

③ After baking, put proper amount of desiccant to seal packages.

1-5. The actual number of module vacuum packing which is based on the actual number of packages to the customer requirements.

2. Module reel packaging items as follows.

2-1. Storage life：12 months. Storage conditions:<40 . Relative ℃ humidity:<90%R.H.

2-2. Module apart packing after 168 hours，To launch patch need to bake, to remove the module hygroscopic, baking temperature conditions：125℃，8hours.

2-3. The actual number of module reel packing which is based on the actual number of packages to the customer requirements.

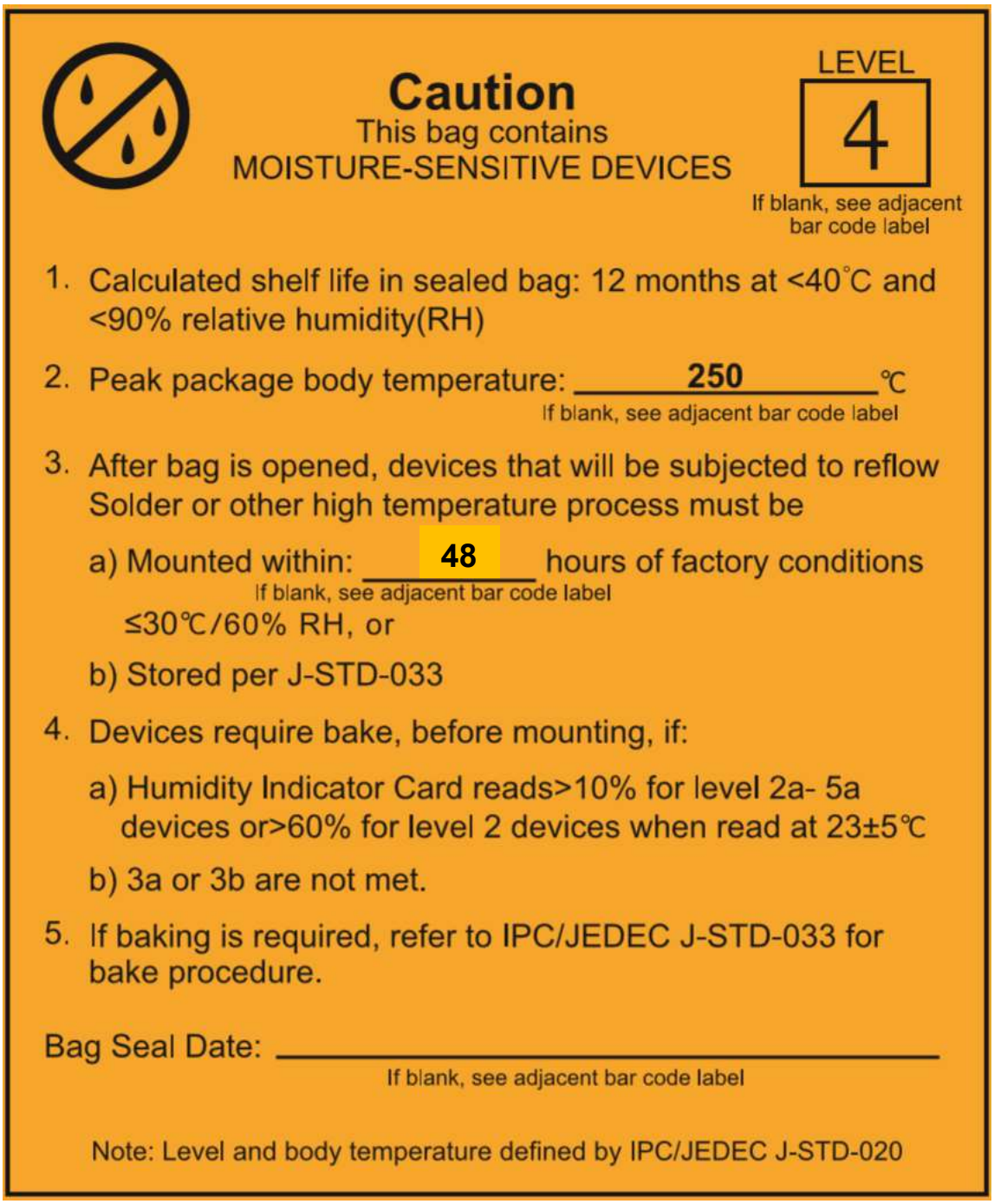
3. Module pallet packaging items as follows：

3-1. Storage life：3 months. Storage conditions:<40 . Relative ℃ humidity:<90%R.H.

3-2. Module if not used within 48 hours, before launch the need for baking, baking temperature: 125 , 8 hours. ℃

3-3. Pallet packaging each plate is 100 PCS.The actual number of module pallet packing which is based on the actual number of packages to the customer requirements.

12. MSL Level / Storage Condition



※NOTE : Accumulated baking time should not exceed 96hrs